

# 74HC173; 74HCT173

Quad D-type flip-flop; positive-edge trigger; 3-state

Rev. 4 — 25 January 2021

Product data sheet

## 1. General description

The 74HC173; 74HCT173 is a quad positive-edge triggered D-type flip-flop. The device features clock (CP), master reset (MR), two input enable ( $\overline{E}1$ ,  $\overline{E}2$ ) and two output enable ( $\overline{OE}1$ ,  $\overline{OE}2$ ) inputs. When the input enables are LOW, the outputs Qn will assume the state of their corresponding Dn inputs that meet the set-up and hold time requirements on the LOW-to-HIGH clock (CP) transition. A HIGH on either input enable will cause the device to go into a hold mode, outputs hold their previous state independently of clock and data inputs. A HIGH on MR forces the outputs LOW independently of clock and data inputs. A HIGH on either output enable pin causes the outputs to assume a high-impedance OFF-state. Operation of the output enable inputs does not affect the state of the flip-flops. Inputs include clamp diodes. This enables the use of current limiting resistors to interface inputs to voltages in excess of  $V_{CC}$ .

## 2. Features and benefits

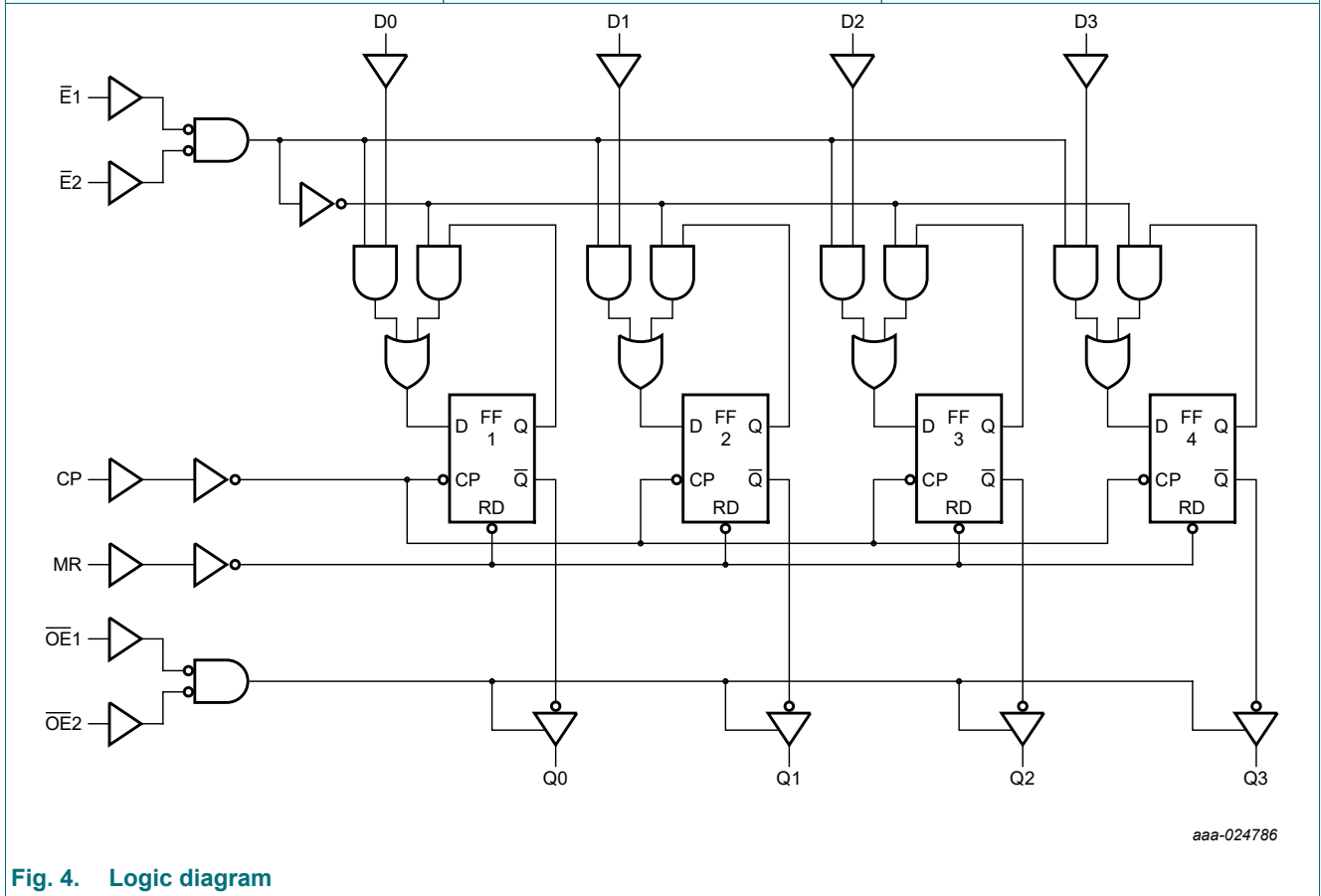
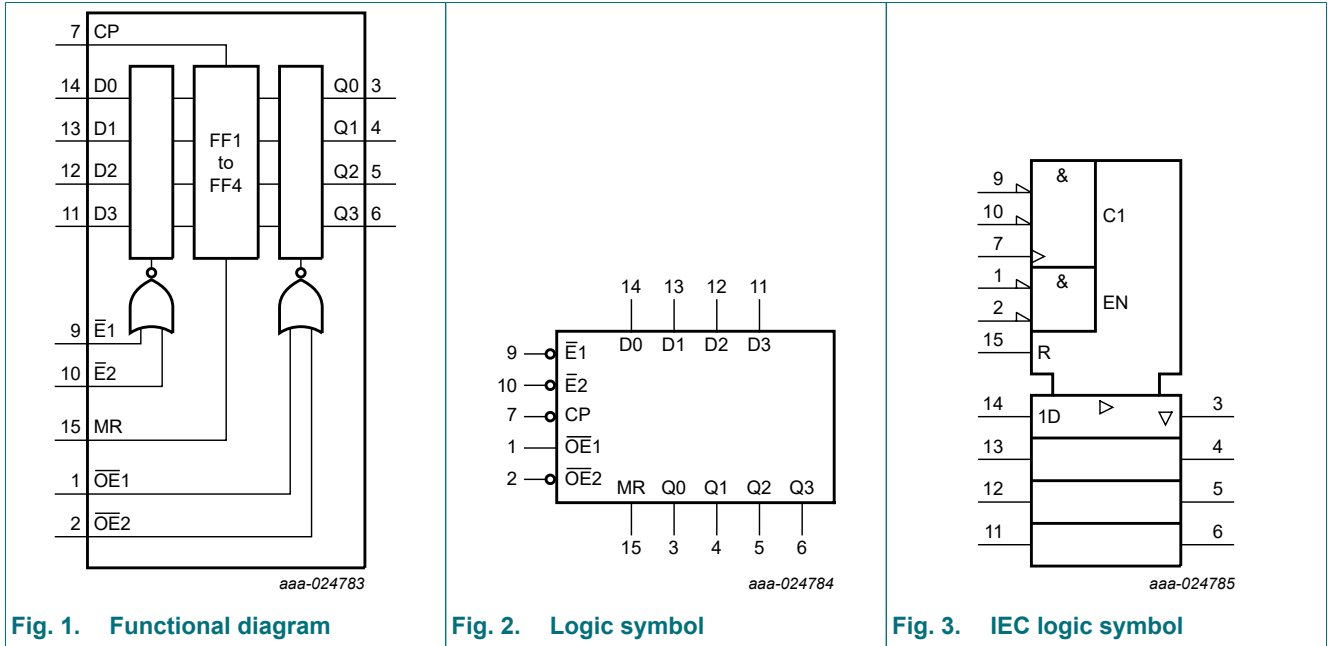
- Complies with JEDEC standard no. 7A
- Input levels:
  - For 74HC173: CMOS level
  - For 74HCT173: TTL level
- Gated input enable for hold (do nothing) mode
- Gated output enable control mode
- Edge-triggered D-type register
- Asynchronous master reset
- ESD protection:
  - HBM JESD22-A114F exceeds 2000 V
  - MM JESD22-A115-A exceeds 200 V
- Specified from -40 °C to +85 °C and -40 °C to +125 °C

## 3. Ordering information

Table 1. Ordering information

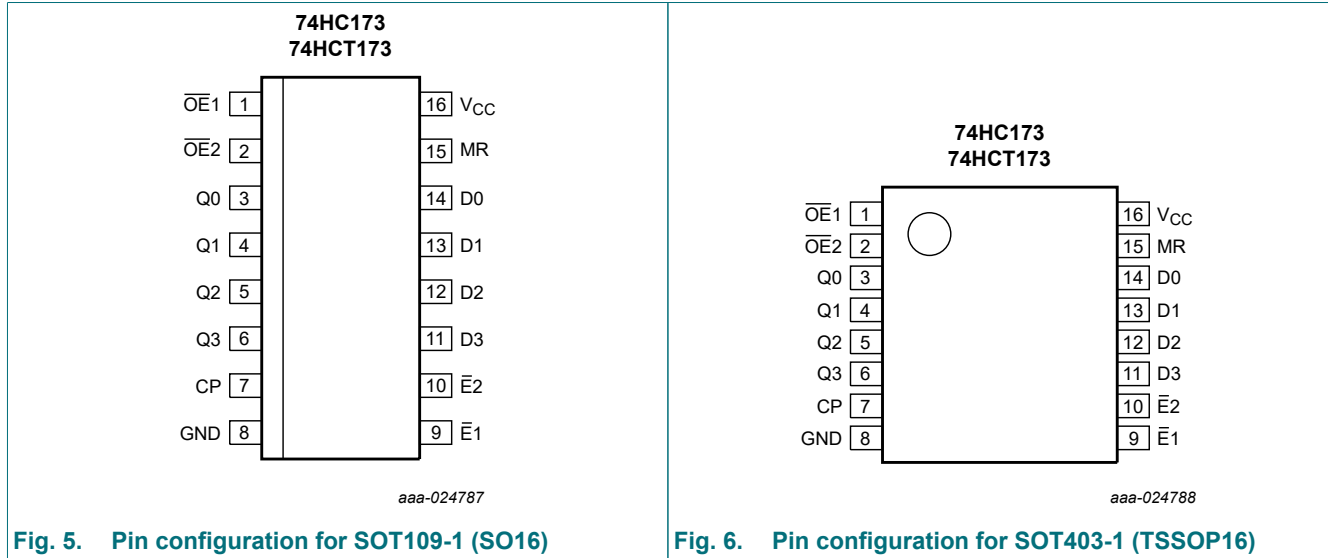
Type number	Package			
	Temperature range	Name	Description	Version
74HC173D	-40 °C to +125 °C	SO16	plastic small outline package; 16 leads; body width 3.9 mm	SOT109-1
74HCT173D				
74HC173PW	-40 °C to +125 °C	TSSOP16	plastic thin shrink small outline package; 16 leads; body width 4.4 mm	SOT403-1

4. Functional diagram



## 5. Pinning information

### 5.1. Pinning



### 5.2. Pin description

Table 2. Pin description

Symbol	Pin	Description
$\overline{OE}1, \overline{OE}2$	1, 2	output enable input (active LOW)
Q0, Q1, Q2, Q3	3, 4, 5, 6	3-state flip-flop output
CP	7	clock input (LOW-to-HIGH, edge triggered)
GND	8	ground (0 V)
$\overline{E}1, \overline{E}2$	9, 10	data enable input (active LOW)
D0, D1, D2, D3	14, 13, 12, 11	data input
MR	15	asynchronous master reset (active HIGH)
V <sub>CC</sub>	16	supply voltage

## 6. Functional description

**Table 3. Function table**

*H = HIGH voltage level; h = HIGH voltage level one set-up time prior to the LOW-to-HIGH CP transition;  
L = LOW voltage level; l = LOW voltage level one set-up time prior to the LOW-to-HIGH CP transition;  
q<sub>n</sub> = lower case letters indicate the state of the referenced input (or output) one set-up time prior to the LOW-to-HIGH CP transition; X = don't care; ↑ = LOW-to-HIGH clock transition.*

Register operating mode	Inputs					Outputs
	MR	CP	E1	E2	Dn	Qn (register)
Reset (clear)	H	X	X	X	X	L
Parallel load	L	↑	l	l	l	L
	L	↑	l	l	h	H
Hold (do nothing)	L	X	h	X	X	q <sub>n</sub>
	L	X	X	h	X	q <sub>n</sub>

**Table 4. Function table**

*H = HIGH voltage level; L = LOW voltage level; X = don't care; Z = high impedance OFF-state.*

3-state buffer operating mode	Inputs			Outputs			
	Qn (register)	OE1	OE2	Q0	Q1	Q2	Q3
Read	L	L	L	L	L	L	L
	H	L	L	H	H	H	H
Disabled	X	H	X	Z	Z	Z	Z
	X	X	H	Z	Z	Z	Z

## 7. Limiting values

**Table 5. Limiting values**

*In accordance with the Absolute Maximum Rating System (IEC 60134). Voltages are referenced to GND (ground = 0 V).*

Symbol	Parameter	Conditions	Min	Max	Unit
V <sub>CC</sub>	supply voltage		-0.5	+7.0	V
I <sub>IK</sub>	input clamping current	V <sub>I</sub> < -0.5 V or V <sub>I</sub> > V <sub>CC</sub> + 0.5 V	-	±20	mA
I <sub>OK</sub>	output clamping current	V <sub>O</sub> < -0.5 V or V <sub>O</sub> > V <sub>CC</sub> + 0.5 V	-	±20	mA
I <sub>O</sub>	output current	-0.5 V < V <sub>O</sub> < V <sub>CC</sub> + 0.5 V	-	±35	mA
I <sub>CC</sub>	supply current		-	+70	mA
I <sub>GND</sub>	ground current		-70	-	mA
T <sub>stg</sub>	storage temperature		-65	+150	°C
P <sub>tot</sub>	total power dissipation		[1]	500	mW

- [1] For SOT109-1 (SO16) package: P<sub>tot</sub> derates linearly with 12.4 mW/K above 110 °C.  
For SOT403-1 (TSSOP16) package: P<sub>tot</sub> derates linearly with 8.5 mW/K above 91 °C.

## 8. Recommended operating conditions

**Table 6. Recommended operating conditions**

Voltages are referenced to GND (ground = 0 V)

Symbol	Parameter	Conditions	74HC173			74HCT173			Unit
			Min	Typ	Max	Min	Typ	Max	
V <sub>CC</sub>	supply voltage		2.0	5.0	6.0	4.5	5.0	5.5	V
V <sub>I</sub>	input voltage		0	-	V <sub>CC</sub>	0	-	V <sub>CC</sub>	V
V <sub>O</sub>	output voltage		0	-	V <sub>CC</sub>	0	-	V <sub>CC</sub>	V
T <sub>amb</sub>	ambient temperature		-40	+25	+125	-40	+25	+125	°C
Δt/ΔV	input transition rise and fall rate	V <sub>CC</sub> = 2.0 V	-	-	625	-	-	-	ns/V
		V <sub>CC</sub> = 4.5 V	-	1.67	139	-	1.67	139	ns/V
		V <sub>CC</sub> = 6.0 V	-	-	83	-	-	-	ns/V

## 9. Static characteristics

**Table 7. Static characteristics**

At recommended operating conditions; voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	25 °C			-40 °C to +85 °C		-40 °C to +125 °C		Unit
			Min	Typ	Max	Min	Max	Min	Max	
<b>74HC173</b>										
V <sub>IH</sub>	HIGH-level input voltage	V <sub>CC</sub> = 2.0 V	1.5	1.2	-	1.5	-	1.5	-	V
		V <sub>CC</sub> = 4.5 V	3.15	2.4	-	3.15	-	3.15	-	V
		V <sub>CC</sub> = 6.0 V	4.2	3.2	-	4.2	-	4.2	-	V
V <sub>IL</sub>	LOW-level input voltage	V <sub>CC</sub> = 2.0 V	-	0.8	0.5	-	0.5	-	0.5	V
		V <sub>CC</sub> = 4.5 V	-	2.1	1.35	-	1.35	-	1.35	V
		V <sub>CC</sub> = 6.0 V	-	2.8	1.8	-	1.8	-	1.8	V
V <sub>OH</sub>	HIGH-level output voltage	V <sub>I</sub> = V <sub>IH</sub> or V <sub>IL</sub>								
		I <sub>O</sub> = -20 μA; V <sub>CC</sub> = 2.0 V	1.9	2.0	-	1.9	-	1.9	-	V
		I <sub>O</sub> = -20 μA; V <sub>CC</sub> = 4.5 V	4.4	4.5	-	4.4	-	4.4	-	V
		I <sub>O</sub> = -20 μA; V <sub>CC</sub> = 6.0 V	5.9	6.0	-	5.9	-	5.9	-	V
		I <sub>O</sub> = -6.0 mA; V <sub>CC</sub> = 4.5 V	3.98	4.32	-	3.84	-	3.7	-	V
V <sub>OL</sub>	LOW-level output voltage	V <sub>I</sub> = V <sub>IH</sub> or V <sub>IL</sub>								
		I <sub>O</sub> = 20 μA; V <sub>CC</sub> = 2.0 V	-	0	0.1	-	0.1	-	0.1	V
		I <sub>O</sub> = 20 μA; V <sub>CC</sub> = 4.5 V	-	0	0.1	-	0.1	-	0.1	V
		I <sub>O</sub> = 20 μA; V <sub>CC</sub> = 6.0 V	-	0	0.1	-	0.1	-	0.1	V
		I <sub>O</sub> = 6.0 mA; V <sub>CC</sub> = 4.5 V	-	0.15	0.26	-	0.33	-	0.4	V
I <sub>CC</sub>	supply current	V <sub>I</sub> = V <sub>CC</sub> or GND; I <sub>O</sub> = 0 A; V <sub>CC</sub> = 6.0 V	-	-	8	-	80	-	160	μA
		V <sub>I</sub> = V <sub>CC</sub> or GND; V <sub>O</sub> = V <sub>CC</sub> or GND	-	-	±0.5	-	±5.0	-	±10	μA
I <sub>I</sub>	input leakage current	V <sub>I</sub> = V <sub>CC</sub> or GND; V <sub>CC</sub> = 6.0 V	-	-	±0.1	-	±1.0	-	±1.0	μA

## Quad D-type flip-flop; positive-edge trigger; 3-state

Symbol	Parameter	Conditions	25 °C			-40 °C to +85 °C		-40 °C to +125 °C		Unit
			Min	Typ	Max	Min	Max	Min	Max	
C <sub>I</sub>	input capacitance		-	3.5	-	-	-	-	-	pF
<b>74HCT173</b>										
V <sub>IH</sub>	HIGH-level input voltage	V <sub>CC</sub> = 4.5 V to 5.5 V	2.0	1.6	-	2.0	-	2.0	-	V
V <sub>IL</sub>	LOW-level input voltage	V <sub>CC</sub> = 4.5 V to 5.5 V	-	1.2	0.8	-	0.8	-	0.8	V
V <sub>OH</sub>	HIGH-level output voltage	V <sub>I</sub> = V <sub>IH</sub> or V <sub>IL</sub> ; V <sub>CC</sub> = 4.5 V								
		I <sub>O</sub> = -20 µA	4.4	4.5	-	4.4	-	4.4	-	V
		I <sub>O</sub> = -6.0 mA	3.98	4.32	-	3.84	-	3.7	-	V
V <sub>OL</sub>	LOW-level output voltage	V <sub>I</sub> = V <sub>IH</sub> or V <sub>IL</sub> ; V <sub>CC</sub> = 4.5 V								
		I <sub>O</sub> = 20 µA	-	0	0.1	-	0.1	-	0.1	V
		I <sub>O</sub> = 6.0 mA	-	0.16	0.26	-	0.33	-	0.4	V
I <sub>I</sub>	input leakage current	V <sub>I</sub> = V <sub>CC</sub> or GND; V <sub>CC</sub> = 5.5 V	-	-	±0.1	-	±1.0	-	±1.0	µA
I <sub>OZ</sub>	OFF-state output current	V <sub>I</sub> = V <sub>IH</sub> or V <sub>IL</sub> ; V <sub>CC</sub> = 5.5 V; V <sub>O</sub> = V <sub>CC</sub> or GND	-	-	±0.5	-	±5.0	-	±10	µA
I <sub>CC</sub>	supply current	V <sub>I</sub> = V <sub>CC</sub> or GND; I <sub>O</sub> = 0 A; V <sub>CC</sub> = 5.5 V	-	-	8.0	-	80	-	160	µA
ΔI <sub>CC</sub>	additional supply current	per input pin; V <sub>I</sub> = V <sub>CC</sub> - 2.1 V; other inputs at V <sub>CC</sub> or GND; V <sub>CC</sub> = 4.5 V to 5.5 V; I <sub>O</sub> = 0 A								
		$\overline{OE}1, \overline{OE}2$	-	50	180	-	225	-	245	µA
		MR	-	60	216	-	270	-	294	µA
		$\overline{E}1, \overline{E}2$	-	40	144	-	180	-	196	µA
		Dn	-	25	90	-	112.5	-	122.5	µA
		CP	-	100	360	-	450	-	490	µA
C <sub>I</sub>	input capacitance		-	3.5	-	-	-	-	-	pF

## 10. Dynamic characteristics

**Table 8. Dynamic characteristics**

Voltages are referenced to GND (ground = 0 V);  $C_L = 50$  pF unless otherwise specified; for test circuit see Fig. 11.

Symbol	Parameter	Conditions	25 °C			-40 °C to +85 °C		-40 °C to +125 °C		Unit
			Min	Typ	Max	Min	Max	Min	Max	
<b>74HC173</b>										
$t_{pd}$	propagation delay	CP to Qn; see Fig. 7 [1]								
		$V_{CC} = 2.0$ V	-	55	175	-	220	-	265	ns
		$V_{CC} = 4.5$ V	-	20	35	-	44	-	53	ns
		$V_{CC} = 5.0$ V; $C_L = 15$ pF	-	17	-	-	-	-	-	ns
		$V_{CC} = 6.0$ V	-	16	30	-	37	-	45	ns
$t_{PHL}$	HIGH to LOW propagation delay	MR to Qn; see Fig. 8								
		$V_{CC} = 2.0$ V	-	44	150	-	190	-	225	ns
		$V_{CC} = 4.5$ V	-	16	30	-	38	-	45	ns
		$V_{CC} = 5.0$ V; $C_L = 15$ pF	-	13	-	-	-	-	-	ns
		$V_{CC} = 6.0$ V	-	13	26	-	33	-	38	ns
$t_{en}$	enable time	$\overline{O}E_n$ to Qn; see Fig. 9 [2]								
		$V_{CC} = 2.0$ V	-	52	150	-	190	-	225	ns
		$V_{CC} = 4.5$ V	-	19	30	-	38	-	45	ns
		$V_{CC} = 6.0$ V	-	15	26	-	33	-	38	ns
$t_{dis}$	disable time	$\overline{O}E_n$ to Qn; see Fig. 9 [3]								
		$V_{CC} = 2.0$ V	-	52	150	-	190	-	225	ns
		$V_{CC} = 4.5$ V	-	19	30	-	38	-	45	ns
		$V_{CC} = 6.0$ V	-	15	26	-	33	-	38	ns
$t_t$	transition time	see Fig. 7 [4]								
		$V_{CC} = 2.0$ V	-	14	60	-	75	-	90	ns
		$V_{CC} = 4.5$ V	-	5	12	-	15	-	18	ns
		$V_{CC} = 6.0$ V	-	4	10	-	13	-	15	ns
$t_w$	pulse width	CP HIGH or LOW; see Fig. 7								
		$V_{CC} = 2.0$ V	80	14	-	100	-	120	-	ns
		$V_{CC} = 4.5$ V	16	5	-	20	-	24	-	ns
		$V_{CC} = 6.0$ V	14	4	-	17	-	20	-	ns
		MR HIGH; see Fig. 8								
		$V_{CC} = 2.0$ V	80	14	-	100	-	120	-	ns
		$V_{CC} = 4.5$ V	16	5	-	20	-	24	-	ns
$V_{CC} = 6.0$ V	14	4	-	17	-	20	-	ns		
$t_{rec}$	recovery time	MR to CP; see Fig. 8								
		$V_{CC} = 2.0$ V	60	-8	-	75	-	90	-	ns
		$V_{CC} = 4.5$ V	12	-3	-	15	-	18	-	ns
		$V_{CC} = 6.0$ V	10	-2	-	13	-	15	-	ns

## Quad D-type flip-flop; positive-edge trigger; 3-state

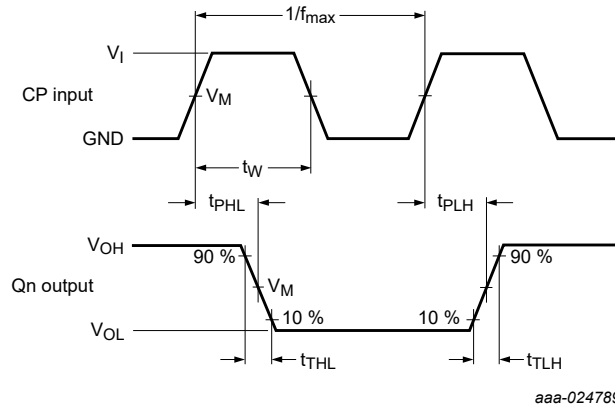
Symbol	Parameter	Conditions	25 °C			-40 °C to +85 °C		-40 °C to +125 °C		Unit
			Min	Typ	Max	Min	Max	Min	Max	
t <sub>su</sub>	set-up time	$\bar{E}n$ to CP; see Fig. 10								
		V <sub>CC</sub> = 2.0 V	100	33	-	125	-	150	-	ns
		V <sub>CC</sub> = 4.5 V	20	12	-	25	-	30	-	ns
		V <sub>CC</sub> = 6.0 V	17	10	-	21	-	26	-	ns
		Dn to CP; see Fig. 10								
		V <sub>CC</sub> = 2.0 V	60	17	-	75	-	90	-	ns
		V <sub>CC</sub> = 4.5 V	12	6	-	15	-	18	-	ns
V <sub>CC</sub> = 6.0 V	10	5	-	13	-	15	-	ns		
t <sub>h</sub>	hold time	$\bar{E}n$ to CP; see Fig. 10								
		V <sub>CC</sub> = 2.0 V	0	-17	-	0	-	0	-	ns
		V <sub>CC</sub> = 4.5 V	0	-6	-	0	-	0	-	ns
		V <sub>CC</sub> = 6.0 V	0	-5	-	0	-	0	-	ns
		Dn to CP; see Fig. 10								
		V <sub>CC</sub> = 2.0 V	1	-11	-	1	-	1	-	ns
		V <sub>CC</sub> = 4.5 V	1	-4	-	1	-	1	-	ns
V <sub>CC</sub> = 6.0 V	1	-3	-	1	-	1	-	ns		
f <sub>max</sub>	maximum frequency	CP; see Fig. 7								
		V <sub>CC</sub> = 2.0 V	6	26	-	4.8	-	4	-	MHz
		V <sub>CC</sub> = 4.5 V	30	80	-	24	-	20	-	MHz
		V <sub>CC</sub> = 5.0 V; C <sub>L</sub> = 15 pF	-	88	-	-	-	-	-	MHz
		V <sub>CC</sub> = 6.0 V	35	95	-	28	-	24	-	MHz
C <sub>PD</sub>	power dissipation capacitance	V <sub>I</sub> = GND to V <sub>CC</sub> ; V <sub>CC</sub> = 5 V; [5] f <sub>i</sub> = 1 MHz	-	20	-	-	-	-	-	pF

Symbol	Parameter	Conditions	25 °C			-40 °C to +85 °C		-40 °C to +125 °C		Unit
			Min	Typ	Max	Min	Max	Min	Max	
<b>74HCT173</b>										
$t_{pd}$	propagation delay	CP to Qn; see Fig. 7 [1]								
		$V_{CC} = 4.5\text{ V}$	-	20	40	-	50	-	60	ns
		$V_{CC} = 5.0\text{ V}; C_L = 15\text{ pF}$	-	17	-	-	-	-	-	ns
$t_{PHL}$	HIGH to LOW propagation delay	MR to Qn; see Fig. 8								
		$V_{CC} = 4.5\text{ V}$	-	20	37	-	46	-	56	ns
		$V_{CC} = 5.0\text{ V}; C_L = 15\text{ pF}$	-	17	-	-	-	-	-	ns
$t_{en}$	enable time	$\overline{OEn}$ to Qn; $V_{CC} = 4.5\text{ V}$ ; see Fig. 9 [2]	-	20	35	-	44	-	53	ns
$t_{dis}$	disable time	$\overline{OEn}$ to Qn; $V_{CC} = 4.5\text{ V}$ ; see Fig. 9 [3]	-	19	30	-	38	-	45	ns
$t_t$	transition time	$V_{CC} = 4.5\text{ V}$ ; see Fig. 7 [4]	-	5	12	-	15	-	19	ns
$t_W$	pulse width	CP HIGH or LOW; $V_{CC} = 4.5\text{ V}$ ; see Fig. 7	16	7	-	20	-	24	-	ns
		MR HIGH; $V_{CC} = 4.5\text{ V}$ ; see Fig. 8	15	6	-	19	-	22	-	ns
$t_{rec}$	recovery time	MR to CP; $V_{CC} = 4.5\text{ V}$ ; see Fig. 8	12	-2	-	15	-	18	-	ns
$t_{su}$	set-up time	$\overline{En}$ to CP; $V_{CC} = 4.5\text{ V}$ ; see Fig. 10	22	13	-	28	-	33	-	ns
		Dn to CP; $V_{CC} = 4.5\text{ V}$ ; see Fig. 10	12	7	-	15	-	18	-	ns
$t_h$	hold time	$\overline{En}$ to CP; $V_{CC} = 4.5\text{ V}$ ; see Fig. 10	0	-6	-	0	-	0	-	ns
		Dn to CP; $V_{CC} = 4.5\text{ V}$ ; see Fig. 10	0	-3	-	0	-	0	-	ns
$f_{max}$	maximum frequency	CP; see Fig. 7								
		$V_{CC} = 4.5\text{ V}$	30	80	-	24	-	20	-	MHz
		$V_{CC} = 5.0\text{ V}; C_L = 15\text{ pF}$	-	88	-	-	-	-	-	MHz
$C_{PD}$	power dissipation capacitance	$V_I = \text{GND to } V_{CC} - 1.5\text{ V}; V_{CC} = 5\text{ V}; f_i = 1\text{ MHz}$ [5]	-	20	-	-	-	-	-	pF

- [1]  $t_{pd}$  is the same as  $t_{PHL}$  and  $t_{PLH}$ .  
 [2]  $t_{en}$  is the same as  $t_{PZH}$  and  $t_{PZL}$ .  
 [3]  $t_{dis}$  is the same as  $t_{PHZ}$  and  $t_{PLZ}$ .  
 [4]  $t_t$  is the same as  $t_{THL}$  and  $t_{TLH}$ .  
 [5]  $C_{PD}$  is used to determine the dynamic power dissipation ( $P_D$  in  $\mu\text{W}$ ):  

$$P_D = C_{PD} \times V_{CC}^2 \times f_i \times N + \Sigma(C_L \times V_{CC}^2 \times f_o)$$
 where:  
 $f_i$  = input frequency in MHz;  
 $f_o$  = output frequency in MHz;  
 $C_L$  = output load capacitance in pF;  
 $V_{CC}$  = supply voltage in V;  
 $N$  = number of inputs switching;  
 $\Sigma(C_L \times V_{CC}^2 \times f_o)$  = sum of outputs.

10.1. Waveforms and test circuit

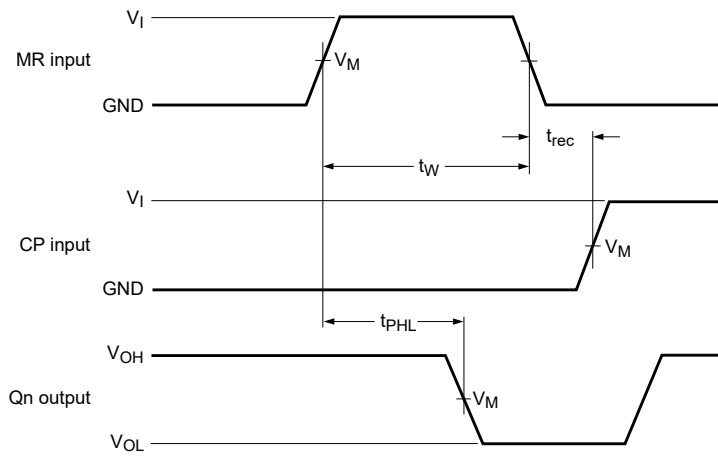


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Measurement points are given in [Table 9](#).

Logic levels  $V_{OL}$  and  $V_{OH}$  are typical output voltage levels that occur with the output load.

**Fig. 7. The clock (CP) to outputs (Qn) propagation delays, clock pulse width, output transition times and maximum frequency**

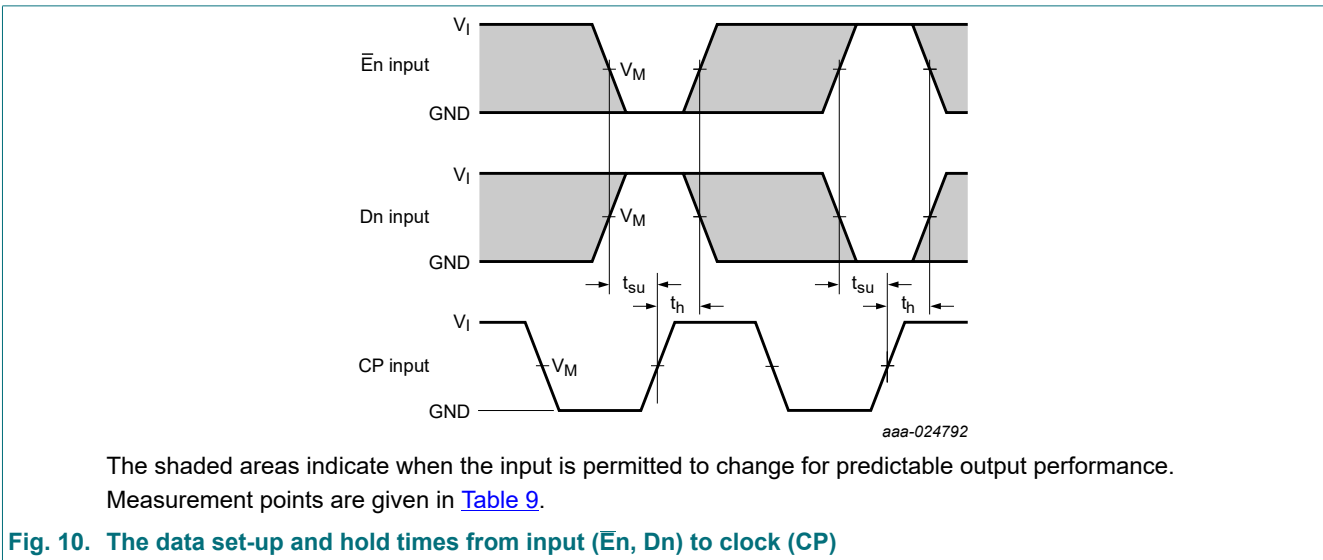
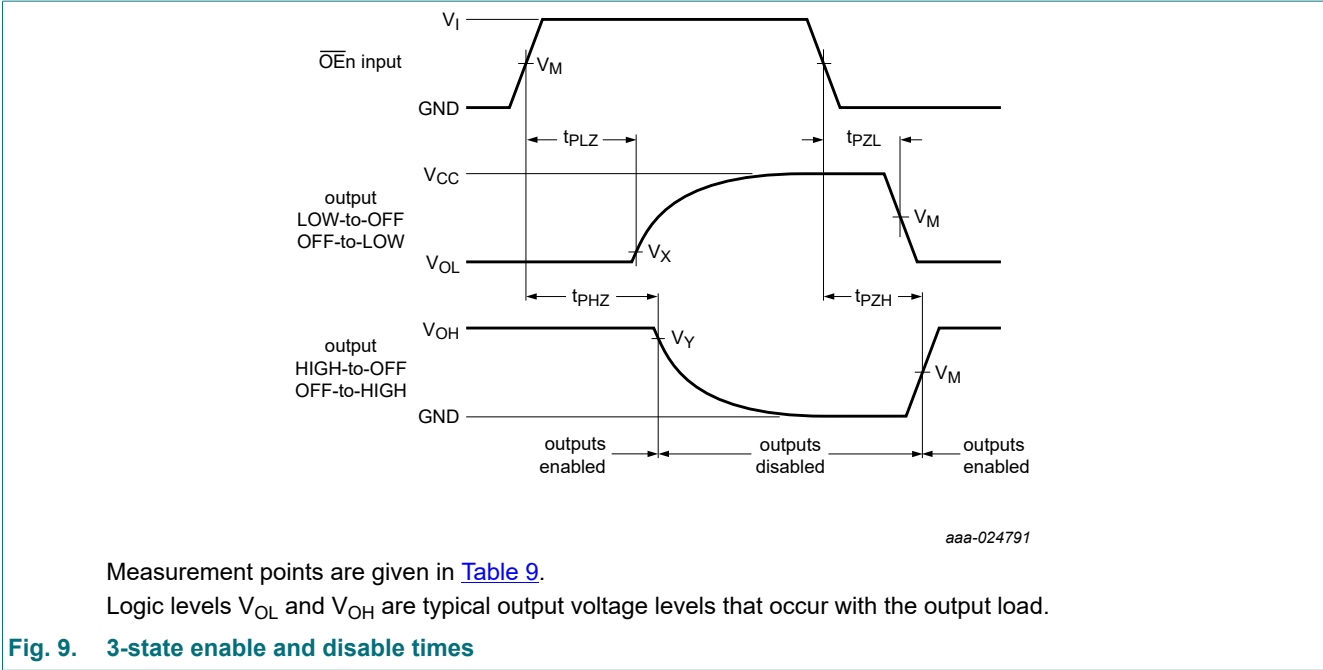


aaa-024790

Measurement points are given in [Table 9](#).

Logic levels  $V_{OL}$  and  $V_{OH}$  are typical output voltage levels that occur with the output load.

**Fig. 8. The master reset (MR) pulse width, master reset to output (Qn) propagation delays, and the master reset to clock (CP) recovery times**



**Table 9. Measurement points**

Type	Input	Output		
	$V_M$	$V_M$	$V_X$	$V_Y$
74HC173	$0.5 \times V_{CC}$	$0.5 \times V_{CC}$	$0.1 \times V_{CC}$	$0.9 \times V_{CC}$
74HCT173	1.3 V	1.3 V	$0.1 \times V_{CC}$	$0.9 \times V_{CC}$

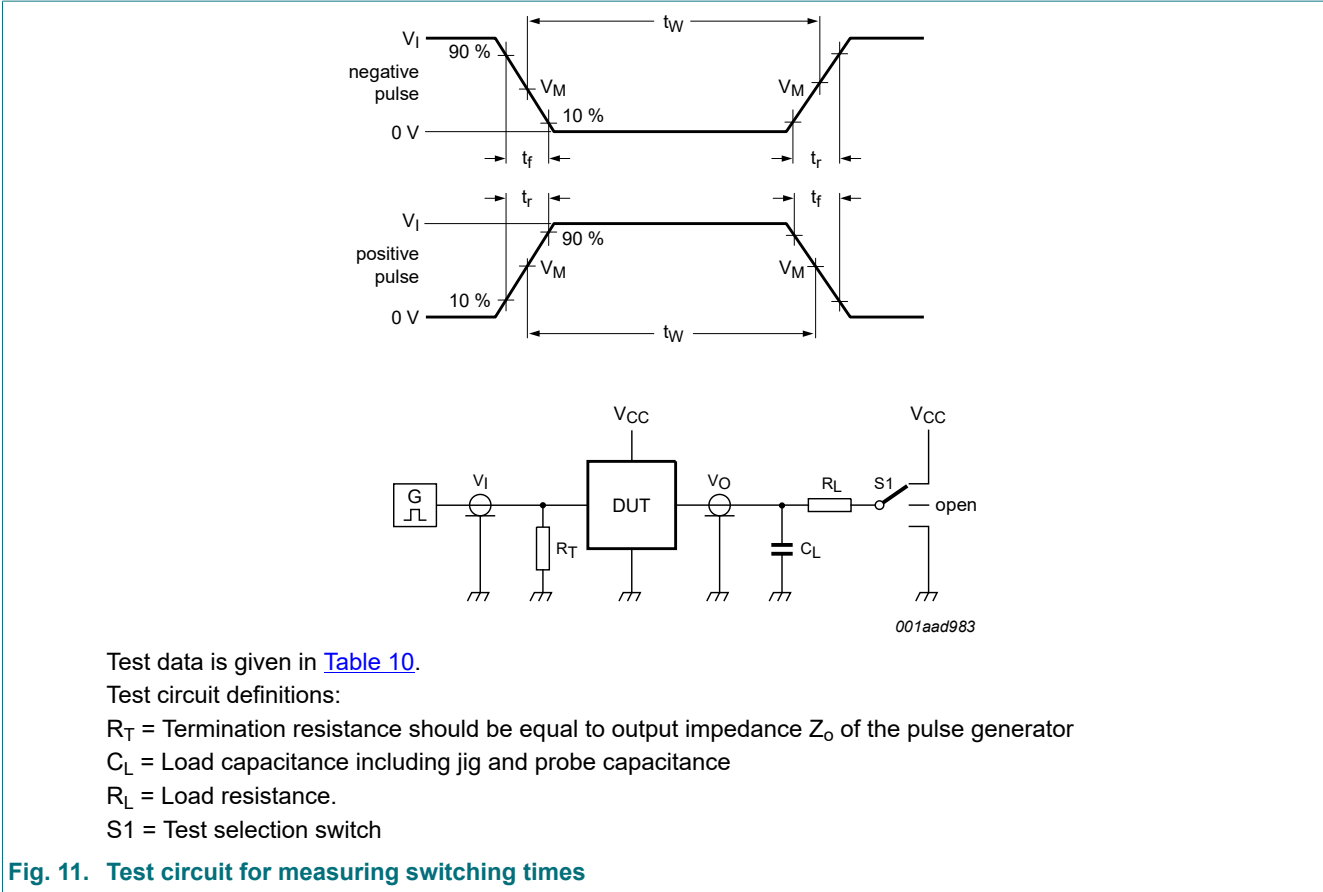


Fig. 11. Test circuit for measuring switching times

Table 10. Test data

Type	Input		Load		S1 position		
	$V_I$	$t_r, t_f$	$C_L$	$R_L$	$t_{PHL}, t_{PLH}$	$t_{PZH}, t_{PHZ}$	$t_{PZL}, t_{PLZ}$
74HC173	$V_{CC}$	6 ns	15 pF, 50 pF	1 k $\Omega$	open	GND	$V_{CC}$
74HCT173	3 V	6 ns	15 pF, 50 pF	1 k $\Omega$	open	GND	$V_{CC}$

11. Package outline

SO16: plastic small outline package; 16 leads; body width 3.9 mm

SOT109-1

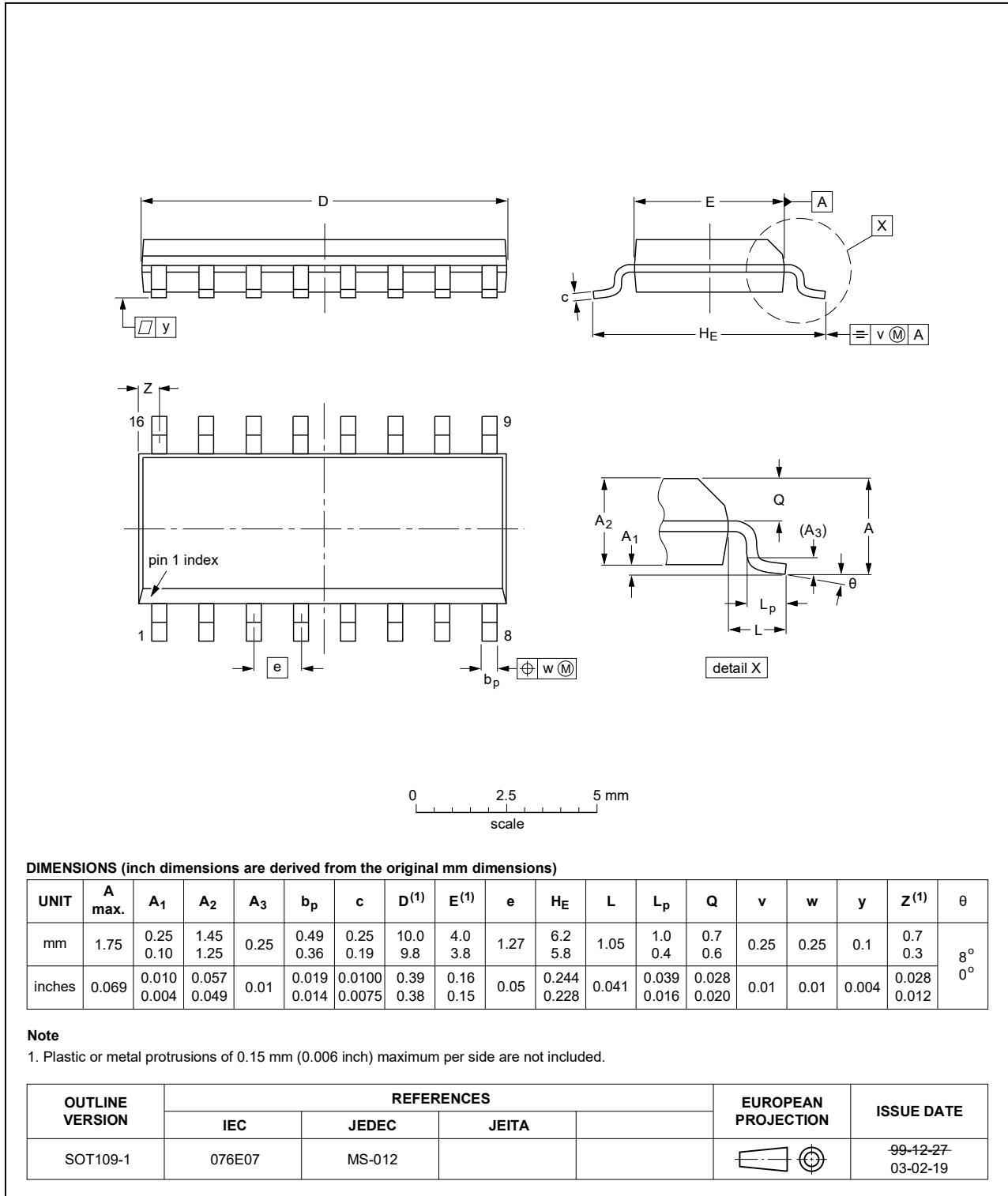


Fig. 12. Package outline SOT109-1 (SO16)

TSSOP16: plastic thin shrink small outline package; 16 leads; body width 4.4 mm

SOT403-1

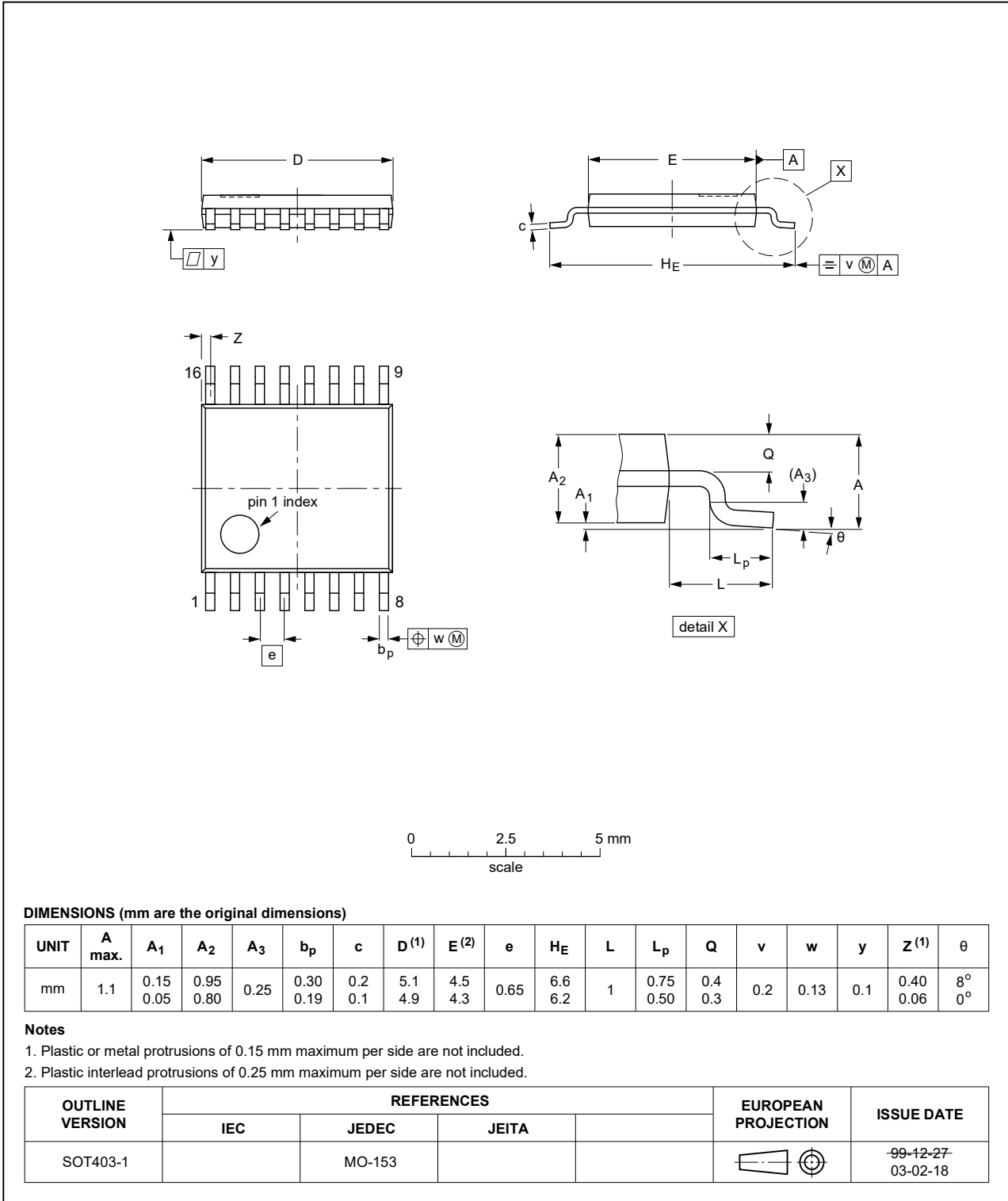


Fig. 13. Package outline SOT403-1 (TSSOP16)

## 12. Abbreviations

Table 11. Abbreviations

Acronym	Description
CMOS	Complementary Metal-Oxide Semiconductor
DUT	Device Under Test
ESD	ElectroStatic Discharge
HBM	Human Body Model
MM	Machine Model
TTL	Transistor-Transistor Logic

## 13. Revision history

Table 12. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
74HC_HCT173 v.4	20210125	Product data sheet	-	74HC_HCT173 v.3
Modifications:	<ul style="list-style-type: none"> <li>The format of this data sheet has been redesigned to comply with the identity guidelines of Nexperia.</li> <li>Legal texts have been adapted to the new company name where appropriate.</li> <li>Type numbers 74HC173DB and 74HCT173DB (SOT338-1/SSOP16) removed.</li> <li><a href="#">Section 7</a>: Derating values for <math>P_{tot}</math> total power dissipation have been updated.</li> </ul>			
74HC_HCT173 v.3	20161108	Product data sheet	-	74HC_HCT173 v.2
Modifications:	<ul style="list-style-type: none"> <li>The format of this data sheet has been redesigned to comply with the new identity guidelines of NXP Semiconductors.</li> <li>Legal texts have been adapted to the new company name where appropriate.</li> <li>Type numbers 74HCT173N and 74HC173N removed.</li> </ul>			
74HC_HCT173 v.2	19901201	Product specification	-	-

## Quad D-type flip-flop; positive-edge trigger; 3-state

## 14. Legal information

### Data sheet status

Document status [1][2]	Product status [3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

- [1] Please consult the most recently issued document before initiating or completing a design.
- [2] The term 'short data sheet' is explained in section "Definitions".
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